

#5/Election
4/10/02
3/14/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Yamazaki, et al. Art Unit : 2823
Serial No.: 09/635,832 Examiner : Fernando Toledo
Filed : August 9, 2000
Title : SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD
THEREFOR

Commissioner for Patents
Washington, D.C. 20231

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RESPONSE

In response to the action mailed September 27, 2001, please amend the application as follows:

In the claims:

Please elect Group I, claims 18-37 and 39-40.

Please amend claim 18-20, 23, 25, and 28-37 as follows:

18. (Amended) An integrated circuit comprising:
a CMOS circuit; [having]
an n-channel field effect transistor and a p-channel
field effect transistor in the CMOS circuit;
said n-channel field effect transistor comprising:
a crystalline semiconductor formed on an
insulating surface;
a source region, a drain region and a channel
forming region in the crystalline semiconductor;
a gate insulating film;

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468.00 DP

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I hereby certify under 37 CFR §1.8(a) that this
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